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# UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. **TESSERA 3.0-102 II DIV**  
First Inventor or Application Identifier **Thomas H. DiStefano**  
Title **PACKAGED MICROELECTRONIC ELEMENT. . .**  
Express Mail Label No. **: EL479140056US**

## APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☒ \* Fee Transmittal Form (e.g., PTO/SB/17)  
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages **32**]  
(preferred arrangement set forth below)
  - Descriptive title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets **6**]
4. Oath or Declaration [Total Pages **2**]
  - a. ☐ Newly executed (original or copy)
  - b. ☒ Copy from a prior application (37 C.F.R. § 1.63(d))  
(for continuation/divisional with Box 16 completed)
    - i. ☐ **DELETION OF INVENTOR(S)**  
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

\* NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. ☐ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
  - a. ☐ Computer Readable Copy
  - b. ☐ Paper Copy (identical to computer copy)
  - c. ☐ Statement verifying identity of above copies

## ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney
9. ☐ English Translation Document (if applicable)
10. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)  
(Should be specifically itemized)
  - \* Small Entity ☐ Statement filed in prior application, Status still proper and desired (PTO/SB/09-12)
13. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
14. ☐ Other: \_\_\_\_\_
15. ☐ Other: \_\_\_\_\_

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment

☐ Continuation ☒ Divisional ☐ Continuation-in-part (CIP) of prior application No: **08 / 962,988**

Prior application information: Examiner **D. Graybill** Group / Art Unit **2814**

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

## 17. CORRESPONDENCE ADDRESS

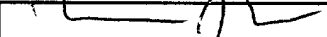
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PACKAGED MICROELECTRONIC ELEMENTS  
WITH ENHANCED THERMAL CONDUCTION

## CROSS REFERENCE TO RELATED APPLICATIONS

5           The present application is a divisional of United  
States Patent Application 08/962,988, filed  
October 31, 1997 the disclosure of which is hereby  
incorporated by reference herein. The present application  
claims benefit of United States Provisional Application No.  
10 60/030,541, filed October 31, 1996 and United States  
Provisional Application No. 60/038,129, filed March 3,  
1997, the disclosures of which are hereby incorporated by  
reference herein.

## 15 FIELD OF THE INVENTION

          The present invention relates to the art of  
electronic packaging and more specifically relates to  
assemblies incorporating microelectronic devices such as  
20 semiconductor chips, methods of making such assemblies, and  
components for making the same.

          Modern electronic devices utilize semiconductor  
integrated circuits or "chips" which incorporate numerous  
electronic components. These chips are mounted on  
25 substrates which physically support the chips and  
electrically interconnect each chip with other elements of  
the circuit. The substrate may be a part of a discrete  
chip package used to hold a single chip. Alternatively, in  
a so-called "hybrid circuit" or "module", one or more chips  
30 are mounted to a substrate forming a circuit panel arranged  
to interconnect the chips and the other circuit elements  
mounted on the substrate. In each case, the chip must be  
securely held on the substrate and must be provided with  
reliable electrical interconnection to the substrate. The  
35 electrical interconnections may include numerous

input/output or "I/O" connections for carrying signals and/or power to the chip.

5 The structures utilized to provide the "first level" interconnection between a chip and the substrate should accommodate all of the electrical interconnections in a relatively compact region of the substrate. Moreover, the first level interconnection structures ordinarily are subject to strain caused by thermal cycling as temperatures in the assembly change. The electrical power dissipated  
10 within the chip tends to heat the chip and the substrate, so that temperatures of the chip and substrate rise and fall as the device is turned on and off. Differential thermal expansion of the chip and substrate cause the contacts on the chip to move relative to the connected  
15 electrical contact pads on the substrate during each heating and cooling cycle of the chip ("thermal cycling"). This tends to cause fatigue of the elements connecting individual contacts and contact pads.

20 The chip package should be capable of dissipating the heat generated by operation so as to limit the temperature rise of the chip. Additionally, the chip package should provide physical protection to the chip and to the electrical connections between the chip and substrate. Thus, the package should protect the chip and  
25 the electrical interconnections from corrosion or other chemical damage. The cost of the chip and the substrate assemblies is also a concern. All of these factors, taken together, present a considerable engineering challenge.

30 One common approach to the chip mounting problem is referred to as a "die attach/wire bond package." The die attach/wire bond package, along with other alternatives, is generally described in Multichip Module-Technologies and Alternatives - The Basics: Doane and Franzon, eds. pp. 56-69. In the die attach/wire bond

process, also referred to as a "face up" wire bond package or simply as a "wire bond" package the chip is placed on a substrate with the contact-bearing front face of the chip facing upwardly, away from the substrate. The rear face of the chip is bonded to the substrate by a material commonly referred to as a die bond material. Fine gold or aluminum wires are connected between individual contacts on the chip and individual contact pads on the substrate. The entire assembly may be contained in an outer package which is filled with an encapsulant or "potting" compound such as a relatively soft silicone or other elastomer. Because the rear face of the chip is connected to the substrate by the die bond adhesive, the wire bond package provides reasonable thermal dissipation from the chip to the substrate. The individual chips must be handled in a "bare" or unpackaged condition during assembly to the substrate. This special handling, and the wire bonding process itself, require considerable care and special operations. However, typical die attach materials having very high thermal conductivity, such as silver or ceramic filled epoxies, are relatively stiff and noncompliant. When a continuous layer of such a material is applied between the chip and the substrate, it can fail during thermal cycling. Further, voids can occur in a layer of die attach material. Gases trapped in voids can cause failure of the package during service. Moreover, it is difficult to test any individual chip at full operating speed before the chip is mounted to the substrate.

As described in PCT International Publication WO 92/05582 and in U.S. Patent 5,347,159, the disclosures of which are incorporated by reference herein, a semiconductor chip assembly may be provided with a flexible, sheet-like backing element overlying the rear face of the chip. Terminals on the backing element are connected to contacts

on the front face of the chip, as by leads extending alongside the edges of the chip. A compliant layer may be provided between the terminals on the backing element and the chip itself, so that the terminals remain movable with respect to the chip. A cover may overlies the front of the chip and may be filled with an encapsulant. The entire assembly may be handled and mounted using essentially the same techniques as are used for surface mounting of conventional components on printed circuit boards. Thus, the terminals of the package can be bonded to contact pads on the substrate using masses of solder disposed between the terminals and contact pads. Prior to mounting, the chip assembly can be tested by engaging a test fixture with the terminals. Such a package typically provides relatively good thermal conductivity between the chip and the package so that the package can serve as a heat sink. However, such a package typically provides limited thermal conductivity between the chip and the substrate.

A chip package sold under the designation Micro-Star BGA by Sharp Corporation and by Texas Instruments, Inc. also includes a chip in a face-up disposition. A flexible polyimide film overlies the back surface of the chip. Wire bonds connect terminals on the front face of the chip to trace terminals on the flexible polyimide film. These terminals in turn can be bonded to a chip by solder balls. A die attach adhesive and a solder mask layer are interposed between the rear face of the chip and polyimide layer. The wire bonds and the chip are covered by a molded epoxy cover. Voids and delaminations in the die attach layer can cause rupture of such a package during thermal cycling. Moreover, such packages typically provide relatively low thermal conductivity from the chip to the substrate.

Additionally, encapsulated metallic conductors such as wire bonds are susceptible to fatigue failures. Typical wire bonds incorporate sharp corners and sharp changes in cross-sectional area at junctions between the fine bonding wire and the connected parts. For example, in a "ball-bond," each fine wire joins a relatively massive ball of wire material at one end. These features tend to create stress concentrations at the junctures. If the wire is flexed repeatedly during service, it can fail at such stress concentrations. Where the wire is encapsulated in a rigid material, differential thermal expansion of the chip and encapsulant can cause repeated flexure of the wire and fatigue failure. Attempts have been made to avoid such fatigue failures by using very soft encapsulants such as soft elastomers or gel. However, these attempts have not been entirely successful; fatigue failure of encapsulated wire bonds remains a significant problem, even with relatively soft encapsulants.

Accordingly, further improvements in microelectronic packaging would be desirable.

#### SUMMARY OF THE INVENTION

The present invention provides such further improvements. One aspect of the present invention provides a semiconductor chip assembly which includes a dielectric element, having top and bottom surfaces such as a flexible, sheetlike element. A semiconductor chip is mounted above the top surface of the dielectric element with the rear surface of the chip facing downwardly towards the dielectric element and with the front surface, bearing contacts, facing upwardly away from the dielectric element. A plurality of thermally conductive elements such as thermally conductive posts are disposed between the top surface of the dielectric element and the rear surface of the chip and most preferably these posts extend all the way

from the top surface of the dielectric element to the rear surface of the chip. The dielectric element has terminals which are accessible from the bottom surface of the dielectric element so that the terminals can be connected to a substrate disposed beneath the dielectric element. Thus, the terminals may be disposed on the bottom surface, or may be accessible from the bottom surface through holes in the dielectric element. Appropriate means are provided for electrically connecting the contacts on the chip to the terminals. For example, flexible leads may extend between the contacts on the chip and conductive traces formed on the dielectric element. Thus, when the terminals are connected to contact pads on the substrate, the chip contacts are electrically connected to the contact pads of the substrate. The posts of the dielectric element and the terminals cooperatively provide a thermal conduction path from the rear face of the chip to the substrate.

Most preferably, the assembly includes a flexible rear encapsulant disposed between the rear surface of the chip and the top surface of the dielectric element, so that the rear encapsulant extends between the posts. The rear encapsulant and the posts preferably fill the space between the rear surface of the chip and the top surface of the dielectric element completely, so that there are no voids in such space. The posts desirably have some flexibility. Thus, the posts may be formed from a material such as a silver-filled epoxy or other metal-filled polymer. Even where a relatively stiff metal-filled polymer or other relatively stiff material is used, the configuration of the posts can be selected to provide reasonable flexibility and hence to permit movement of the dielectric element relative to the rear face of the chip. As discussed below, such relative movability allows compensation for thermal expansion and limits mechanical stresses in the system.

In a particularly preferred arrangement, some or all of the individual posts on the top surface of the dielectric element are disposed directly above corresponding terminals on the bottom surface of the dielectric element, so that each of these posts is directly aligned with the corresponding terminal. The aligned posts and terminals may be electrically connected to one another, or else may be separated from one another by a relatively thin dielectric layer such as a solder mask layer. In either case, the aligned posts and terminals provide a straight, low-resistance thermal path from the rear surface of the chip to the substrate when the terminals are bonded to contact pads on the substrate. In further preferred embodiments, a layer of a highly thermally conductive metal, such as copper, may be provided over the top surface of the dielectric element between the dielectric element and the individual posts to provide enhanced thermal dissipation from the chip to the substrate by providing an additional thermal conduction path. The dielectric element becomes relatively less flexible as the thickness of the layer of highly thermally conductive metal increases. The thermally conductive layer makes alignment of the posts and the solder masses less important because the layer provides horizontal conduction therebetween. The assembly thus provides good thermal dissipation from the chip to the substrate. This thermal dissipation is further aided by the rear encapsulant, which provides further thermal conductivity between the rear surface of the chip and the top surface of the dielectric element. The rear encapsulant has a thermal conductivity of approximately between about 1.0 to about 10.0 W/cm-°K.

A further aspect of the present invention provides a semiconductor chip assembly which also includes





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A further aspect of the invention provides a microelectronic assembly incorporating a chip or other microelectronic element having a front surface with contacts thereon and having flexible leads such as wire bonds extending from contacts on the front surface of the chip, the leads being connected to the contacts of joints on the front surface. Here again, a lead encapsulant, preferably a flexible encapsulant surrounds the leads and the chip. A spreader is disposed over the front surface of the chip and overlies the contacts and the adjacent regions of the lead encapsulant. Thus, the lead encapsulant extends between the chip front surface and the spreader. The spreader has a coefficient of thermal expansion close to the coefficient of thermal expansion of the chip or other microelectronic element and preferably substantially equal to the coefficient of thermal expansion of the chip. The spreader may serve as a physically protective packaging element and may also help to dissipate heat from the microelectronic element.

The spreader tends to suppress shear strain in the encapsulant in the vicinity of the contacts. Stated another way, expansion and contraction of the encapsulant are substantially constrained by the confronting surfaces of the microelectronic element and spreader. Upon heating or cooling of the assembly, the encapsulant surrounding each lead in the vicinity of the chip contact tends to move along with the contact. This minimizes shear stress in the lead at the contact. By contrast, if the encapsulant were constrained between a microelectronic element and a packaging element having coefficient of thermal expansion markedly different from that of the microelectronic element, significant shearing can occur in the encapsulant. As the encapsulant deforms in shear, it can impose significant flexural loads on the leads embedded therein.

Such substantial loads can occur even if the encapsulant itself is soft. Indeed, substantial shearing loads can occur even if a soft encapsulant is unconstrained, if the encapsulant itself has a coefficient of thermal expansion  
5 substantially different from that of the microelectronic element.

In certain instances, it may be desirable to modify the shear strain which is present in the lead encapsulant. Thus, in preferred embodiments of the present  
10 invention, changes in the shear strain in the encapsulant in the vicinity of the contacts may be induced by changing the surface area of the spreader or changing the thermal mass of the spreader. For example, the surface area of the spreader confronting the chip contacts may be reduced which  
15 will, in turn, reduce the ability of the spreader to constrain the encapsulant in the vicinity of the contacts. Conversely, the thermal mass of the spreader may be increased to enhance the spreader's ability to constrain the encapsulant in the vicinity of the contacts.  
20 Alternatively, the shear strain in the encapsulant in the vicinity of the contacts may be modified by changing the geometry or shape of the lead encapsulant itself, e.g. forming the encapsulant layer with sloped sidewalls.

A package according to the most preferred  
25 embodiments of the present invention incorporates the features of all of the aspects discussed above.

A further aspect of the invention provides a method of enhancing the reliability of electrical connections in a semiconductor package during operation of  
30 the chip. The method includes the steps of providing a semiconductor chip having a front contact bearing surface and a rear surface; providing flexible leads extending from the contacts on the front surface of the chip, the flexible leads being connected to the contacts at joints on the

front surface; juxtaposing a spreader above the front surface, the spreader having a coefficient of thermal expansion substantially equal to the coefficient of thermal expansion of the chip; and disposing a liquid encapsulant  
5 between the front surface and the spreader and around the leads and curing the encapsulant, whereby the motion of the leads during thermal cycling is constrained.

The foregoing and other objects, features and advantages of the present invention would be more readily  
10 apparent from the detailed description of the preferred embodiments set forth below, taken in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic, partially sectional  
15 view of a microelectronic assembly in accordance with one embodiment of the invention.

Fig. 2 is a fragmentary, diagrammatic sectional view depicting portions of an assembly in accordance with a further embodiment of the invention.

20 Fig. 3 is a view similar to Fig. 2 but depicting portions of an assembly in accordance with yet another embodiment of the invention.

Fig. 4 is a diagrammatic sectional view depicting an assembly in accordance with yet another embodiment of  
25 the invention.

Fig. 5 is a view similar to Fig. 4 but depicting an assembly in accordance with another embodiment of the invention.

Fig. 6 is a diagrammatic, partially sectional  
30 view of a microelectronic assembly in accordance with another embodiment of the present invention.

Fig. 7 is a diagrammatic, partially sectional view of a microelectronic assembly in accordance with yet another embodiment of the present invention.

Fig. 8 is a diagrammatic, partially sectional view of a microelectronic assembly in accordance with still another embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

5 A microelectronic assembly in accordance with one embodiment of the present invention incorporates a dielectric element 20 having a top surface 22 and a bottom surface 24. Dielectric element 20 is formed as a flexible sheet of a dielectric material as, for example, a sheet of  
 10 a polyimide between about 15 and about 40 microns thick and desirably about 25 microns thick. The dielectric element further includes metallic conductive traces 26 disposed on the top surface of the dielectric element. The conductive traces define terminals 28 which are exposed to the bottom  
 15 surface through holes 30 in the dielectric element. Only some of terminals 28 and holes 30 are visible in Fig. 1. The terminals and holes are distributed in an array over substantially the entire sheet or dielectric element 20. Also, only some of the metallic traces 26 are visible in  
 20 Fig. 1. A microelectronic element, in this case a conventional semiconductor chip 32 is disposed above the top surface of the dielectric element. Chip 32 has a top surface 34, bottom surface 36 and edges 38 extending between such surfaces. The chip is substantially  
 25 rectangular and hence has additional edges (not shown) perpendicular to edges 38. Contacts 40 are disposed on the top surface 34 of the chip, in rows parallel to edges 38 and in other rows (not shown) parallel to the additional edges of the chip. The chip also has an electrically  
 30 conductive potential plane 42 on back surface 36. The potential plane is arranged to serve as a ground or power potential reference plane for the internal electronic elements (not shown) incorporated in the chip.

A thin, insulating film such as a conventional solder mask 46 overlies the top surface of the dielectric element and traces 26. Film 46 desirably is less than about 40 microns thick. The film incorporates apertures 48 aligned with a few of the terminals, such as terminal 28a, visible in Fig. 1.

A plurality of thermally conductive flexible posts 50 are disposed between the bottom surface of the chip and the top surface 22 of the dielectric element. Each of the posts 50 is aligned with a terminal 28. For example, post 50b is aligned with terminal 28b. The majority of the posts are supported on insulating film 46. Post 50a, however, is aligned with aperture 48 and hence makes direct electrical contact with the aligned terminal 28a. Posts 50 are formed from a thermally and electrically conductive material. For example, a die attach adhesive such as a silver-filled epoxy of the type sold by Creative Materials, of Tyngsboro, MA under the designation 100-49 can be used. Posts 50 should be flexible enough to accommodate displacements of the magnitude which will be caused by thermal expansion of the chip. That is, the posts 50 should be capable of flexing through a range of movement equal to the maximum expansion of the chip relative to surrounding components. A conservative measure of such maximum movement is the product of the coefficient of thermal expansion of the chip, multiplied by the maximum distance along the lower surface of the chip from the center of the lower surface to the most remote corner; multiplied again by the maximum temperature difference to be encountered in the entire life cycle of the assembly, including manufacturing operations, testing, storage and service. The movement calculated according to this rule typically will be greater than the actual movement encountered in service. The desirable elastic modulus of

the material in the posts will vary with the height of the posts. Preferably, however, the posts are between about 50 and about 250 microns high and the elastic modulus of the material in the posts is less than about one GigaPascals.

5 Preferably, the material in the posts has a thermal conductivity of at least about 1.0 and more preferably at least about 10.0 W/cm-°K. The posts desirably occupy between about 20 to about 60 % of the available area on the back surface of the chip.

10 A plurality of flexible leads 54 extend from contacts 40 on the chip to bond points 56 on the traces 26 of dielectric element 20. The bond points 56 are disposed in rows, in edge regions of the dielectric element disposed outboard of the edges 38 of the chip and outboard of the  
15 other edges (not shown). Thus, each row of contacts 40 along an edge of the chip is connected to a row of bond points 56 along the adjacent edge region of the dielectric element. Leads 54 may be conventional bonding wires, typically gold or aluminum bond wires. Alternatively,  
20 leads 54 may be flat, strip-like leads such as those used in tape automated bonding processes, or leads as disclosed in the aforementioned '582 International Publication. Other types of flexible leads may also be used.

A flexible rear encapsulant 52 occupies the space  
25 between the rear surface 36 of the chip and the top surface 22 of the dielectric layer, completely filling any voids left unoccupied by the posts, insulating layer 46, and traces 26. The rear encapsulant has a thermal conductivity of approximately between about 1.0 to about 10.0 W/cm-°K.  
30 A dielectric lead encapsulant 58 intimately surrounds the leads or bonding wires 54 and covers the top surface 34 of the chip as well as the top surface 22 of the dielectric layer. Lead encapsulant 58 may be of the same composition

as rear encapsulant 52, or else may be a separate material. For example, rear encapsulant 52 may be loaded with a thermally conductive filler, and may be electrically conductive whereas lead encapsulant 58 may be left  
5 unloaded. Desirably, the lead encapsulant and the rear encapsulant are both flexible. The encapsulants may be a gel, an elastomer or other soft, flexible material. The encapsulants desirably have tensile modulus of elasticity or young's modulus less than 100,000 pounds per square inch  
10 (less than 670 MegaPascals) and most desirably between about 100 pounds per square inch and about 10,000 pounds per square inch (between 0.67 and 67 MegaPascals). The encapsulants preferably have hardness below about 60 on the Shore D durometer scale, more preferably between about  
15 Shore A 20 and about Shore D 60 and most preferably between about Shore A 20 and about Shore A 90. Many conventional soft potting compounds utilized in the semiconductor industry can be employed. For example, gels, elastomers, soft epoxies and the like may be used. A silicone gel of  
20 the type sold under the designation 577 by the Dow Corning Corporation of Midland, Michigan may be used. A silicone gel such as the Dow Corning DC6810 silicone gel may be used. Alternatively, a Thermoset 323 flexible epoxy encapsulant may be used.

25 A spreader 60 overlies the lead encapsulant 58 and overlies the front surface 34 of the chip. Spreader 60 is formed from a material having a coefficient of thermal expansion close to that of the chip. Desirably, the linear coefficient of thermal expansion of spreader 60 is between  
30 about 50% and about 200% of the linear coefficient of thermal expansion of the chip. For a conventional silicon chip having a linear coefficient of thermal expansion of about  $3 \times 10^{-6}$  cm/cm-°C, the linear coefficient of thermal



expansion of spreader 60 desirably is between about 1.5 and about  $6 \times 10^{-6}$  cm/cm-°C. Spreader 60 desirably has a relatively high thermal conductivity. Metal alloys such as those commonly referred to as Invar, Copper/Invar, Alloy 42, Tungsten/Copper, Molybdenum and the like can be employed. Preferably, the lead encapsulant 58 is bonded to spreader 60 and chip 32. The lead encapsulant as would be appreciated may, and typically does, have a coefficient of thermal expansion in its free or unconstrained state substantially different from that of the chip. For example, typical silicone encapsulants have linear coefficients of thermal expansion on the order of about 400-600 cm/cm-°C. While it is preferable that the spreader be metallic, other CTE matched materials may be used as well such as silicon and alumina, as well as others.

Electrically and thermally conductive bonding material 62, preferably a metallic bonding material such as conventional solder masses, may be provided on the bottom surfaces of terminals 28 so that the bonding material masses 62 protrude from the bottom surface 24 of the dielectric element. In use, the assembly can be handled, stocked and transported as a unit. Spreader 60 and encapsulant 58 protect the delicate leads 54 and chip 32. The assembly can also be tested as by engaging the solder masses 62 with contacts of a test fixture and actuating the chip. The assembly can be mounted on a conventional substrate such as circuit panel 66 by juxtaposing the solder masses 62 with bonding pads 68 on the substrate and heating the assembly in the conventional manner to melt the solder and then cooling the assembly. These steps may be performed by the same procedures used to mount a conventional surface mounted component. Once mounted in

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this fashion, terminals 28 and hence traces 26, leads 54, and contacts 40 are electrically connected to the contact pads 68 of the substrate. Conductive posts 50a and other, similar posts having contact with terminals 28 electrically  
5 connect the ground or potential plane 42 of the chip with the appropriate ground or power contact pads of the substrate. The remaining posts 50 do not make electrical connections. However, all of the aligned posts 50, terminals 28 and solder masses 62 provide short, low  
10 resistance thermal conduction paths from the bottom surface of the chip to the substrate and thus help to provide effective heat transfer from the chip to the substrate. This limits the temperature rise of the chip.

Several features of the design tend to limit  
15 thermal stresses applied to the leads during mounting and service. Because spreader 60 and chip 32 have similar coefficients of thermal expansion, both tend to expand and contract by approximately the same amounts during temperature changes. That portion of lead encapsulant 58  
20 surrounding contacts 40 and surrounding the adjacent portions of leads 54 is constrained between the spreader and the chip top surface 34. The lead encapsulant in this region thus tends to move with the chip and the spreader. Therefore, there is little, if any, shear strain in the  
25 lead encapsulant in the vicinity of contacts 40 and the adjacent regions of leads 54. Accordingly, the relatively delicate joints between the leads and contacts 40 are effectively protected from flexure during thermal cycling.

Moreover, the dimensions of the parts are  
30 selected so that movement of the bond points 56 on the dielectric layer is substantially equal to the movement of the immediately adjacent portions of the lead encapsulant during thermal expansion and contraction. Movement of the parts of the assembly is discussed herein with reference to

the center of the chip or microelectronic element. Thus, movement of elements in directions to the right and left as seen in Fig. 1 is taken with reference to the medial plane 70, equidistant from edges 38. For the bond points 56 lying alongside edges 38 of the chip, movement of the lead encapsulant surrounding bond points 56 during a given change in temperature is substantially equal to the sum of the movement of edge 38 and the thermal expansion of that portion of the encapsulant lying between edges 38 and bond points 56. That sum is given by

$$D_c \epsilon_c + D_e \epsilon_e \quad (1)$$

where:  $D_c$  is the distance from a given edge 38 to medial plane 70 of the chip;  $\epsilon_c$  is the linear thermal coefficient of expansion of the chip material;  $D_e$  is the distance from edge 38 of the chip to bond point row 56; and  $\epsilon_e$  is the linear coefficient of expansion of the lead encapsulant. The movement of the bond points 58 on the dielectric layer and traces is the product of  $D_d$ , the distance from medial plane 70 to the bond points and  $\epsilon_d$ , the linear coefficient of expansion of the dielectric layer and traces. Typically, the thermal expansion of the metallic traces controls the thermal expansion of the dielectric layer. That is, the coefficient of thermal expansion of the dielectric layer in directions parallel to traces 26 can be taken as equal to the thermal coefficient of expansion of the copper material in the traces, i.e., about  $150 \times 10^{-6}$  cm/cm-°C. Thus, the dimensions are selected so that

$$D_d \epsilon_d = D_c \epsilon_c + D_e \epsilon_e \quad (2)$$

Similar selections are made with respect of the rows bond points adjacent the other edges of the chip (not shown). In each case, the medial plane used as the base of

measurement is the plane parallel to the particular edge of the chip and passing through the geometric center of the chip bottom surface. Thermal expansion matching achieved by selection of dimensions in the foregoing manner does not assure absolute absence of shear at bond points 56. For example, temperatures in the system may vary in a non-uniform manner. Also, when the assembly has been bonded to a substrate, the dielectric layer is bound to the substrate so that expansion and contraction of the substrate may dominate expansion and contraction of the dielectric layer. Preferably, however, the substrate has a coefficient of thermal expansion close to that of the dielectric layer with lead traces thereon. For example, substrate 66 may be another copper and polyimide structure. Moreover, the most severe thermal cycling in the history of the device typically occurs during solder bonding, before the dielectric layer is physically bound to the substrate. Therefore, selection of dimensions in the manner discussed above will provide useful reductions in thermal stress during this critical time.

As shown in Fig. 2, an assembly in accordance with a further embodiment of the invention includes a chip 32' similar to that discussed above having contacts 40' on its top surface, as well as a spreader 60' overlying the contact-bearing top surface of the chip as discussed above. The assembly further includes a dielectric element 20' generally similar to that discussed above with reference to Fig. 1, except that the traces 26' of layer 20' are embedded within the dielectric layer. For example, dielectric element 20' may be a composite structure including two or more dielectric layers laminated together. Traces 26' are exposed to the top surface of the dielectric element at bond points 56' through holes or slots 57' in the top portion of the dielectric element. Accordingly,

there is no need for a separate solder mask layer such as the solder mask layer 46 used in the embodiment of Fig. 1. Here again, posts 50' are aligned with terminals 28' and hence aligned with the bonding material or solder masses 62 applied to the terminals. The aligned posts and terminals provide efficient paths for heat conduction to the bottom of the assembly. Desirably, the thickness of dielectric element 20' is limited so that the thermal resistance between each post 50' and the aligned terminal 28' is small. For example, the thickness of a polyimide layer intervening between posts 50' and terminals 28' desirably is less than 40 microns.

The embodiment illustrated in Fig. 3 is similar, except that the dielectric layer 20'' has traces 26'' both on its top surface and on its bottom surface. Some of the terminals, such as terminal 28a'' are flat structures disposed on the bottom surface 24'' of the dielectric element, whereas other terminals 28b'' include metallic structures such as via liners extending through the thickness of the dielectric element. These metallic structures also enhance the thermal conductivity of the structure in the vertical direction, from the top surface towards the bottom surface. As in the embodiments discussed above with reference to Fig. 1, an additional thin dielectric layer 46'' overlies the top surface of the dielectric element. Here again, apertures can be provided in such layer to connect some of the posts 50'' to traces and/or terminals on the top surface. In each edge region of the dielectric element, the bond points 56 where the flexible leads 54'' join the traces 26'' are disposed in two rows 56a'' and 56b'' extending parallel to edge 38'' of the chip. Thus, some of the leads extending from the contacts 40'' join the traces 26'' on the top surface of the dielectric element at a first row of bond points 56a'',

whereas other leads 54 and traces 26'' on the bottom surface 24'' at bond points 56''. Here again, the dielectric element is provided with one or more apertures, such as one or more elongated slots, to accommodate each row of bond points 56a'' for the lower surface traces. In other respects, the embodiment of Fig. 3 is similar to those discussed above. The multilayer structure of Fig. 3 may incorporate more than two layers of traces and more than two rows of bond points associated with each edge of the chip. For example, a layer of traces extending in the middle of the dielectric element, such as traces 26' discussed above with reference to Fig. 2, may be provided. As would be appreciated, in any such structure which incorporates multiple rows of bond points positioned at different distances  $D_A$  and  $D_B$  from the adjacent edge 38'' of the chip, it is impossible to select both distances to match precisely the desired distance  $D_E$  calculated above. Preferably, both such distances  $D_A$  and  $D_B$  approximate the desired distance  $D_E$ .

The assembly of Fig. 4 is generally similar to the assembly of Fig. 1 discussed above. However, dielectric element 120 has terminals 128a disposed in peripheral regions of the dielectric element, outboard of bond rows 156 in addition to terminals 128b, in the central region beneath chip 132. Thus, the terminals of dielectric element 120 provide a "fan-in" and "fan-out" arrangement. Some of the traces 126a extend outwardly from their bond points 156 to their connected terminals 128a, whereas other traces 126b extend inwardly from their bond points to their connected terminals 128b. A capacitor 110 having a conductive bottom plate 112, conductive top plate 114 and dielectric layer 116 between the top and bottom plates is disposed over the central region of the dielectric element. Thus, thermally conductive posts 150 are separated from the

dielectric element and from terminals 128b by the intervening capacitor. However, the capacitor does not provide a large thermal resistance between the posts and the terminals. Conductive layers 112 and 114 desirably are  
5 metallic and have relatively high thermal conductivity. Dielectric layer 116 typically is less than about 40 microns thick and hence adds little thermal resistance to the structure. A thin dielectric film (not shown) may be provided atop the top conductive layer 114 of the capacitor  
10 to electrically insulate posts 150 from the capacitor if desired. Preferably however, posts 150 remain electrically connected to the top layer 114 of the capacitor so that all of the posts electrically connect the top layer of the capacitor to the potential plane layer 136 on the bottom  
15 surface on chip 132. The conductive layers 112 and 114 of the capacitor are connected to one or more of terminals 128 and desirably are also connected to one or more of the flexible leads 154 which serve as ground and power leads to the chip. For example, trace 126a, as seen in Fig. 4, is  
20 electrically connected to the bottom plate 112. This provides a compact package with on-board capacitance to compensate for inductances in the leads. Two or more capacitors may be provided in the package. These may be stacked atop one another or, preferably, provided alongside  
25 one another. Additional capacitors may be provided over the peripheral regions of the dielectric element, outboard of bond points 156 and overlying the outboard terminals 128a.

In the assembly of Fig. 4, posts 150 are aligned with terminals 128b of the central region in the manner  
30 discussed above, to provide straight, vertical heat conduction paths from chip 132 to the terminals. However, some or all of the posts can be out of alignment with the terminals. The degree of increase in thermal resistance caused by such misalignment depends on the degree of

misalignment or horizontal distance, in the plane of dielectric element 120, from each post to the nearest terminal. The greater such misalignment, the greater the increase in thermal resistance. Preferably, the degree of misalignment or horizontal distance from each post 150 to each terminal 128 is less than about 100 microns. Where metallic elements of the structure, such as the conductive layers 112 and 114 of a capacitor or traces 126 provide substantial thermal conductivity in horizontal directions, the effects of terminal-to-post misalignment are reduced. For example, the capacitor can be provided with a relatively thick metallic top or bottom plate to enhance the thermal conductivity of the dielectric element in horizontal directions parallel to the surfaces of the element.

The assembly of Fig. 4 further includes a thermally conductive plug 161 disposed between the top surface of chip 132 and spreader plate 160. Plug 161 is bonded to both the top surface of the chip and the spreader plate and provides a low-resistance thermal path from the chip to the spreader. This enhances heat dissipation from the chip and also tends to equalize the temperatures of the spreader and chip. This further reduces shear in those regions of the lead encapsulant disposed between the top surface of the chip and the spreader and thus further reduces bending stress in those portions of leads 156 overlying the top surface, such as the lead portions adjacent contacts 140 of the chip.

Packages according to the foregoing embodiments can be fabricated by a process which starts with a preformed dielectric element having the traces and terminals discussed above. If capacitors as discussed above with reference to Fig. 4 are to be provided in the assembly, they may be included in the prefabricated



dielectric element. The dielectric element typically is provided in the form of a tape with features such as sprocket holes and alignment masks (not shown). Posts, such as posts 50 (Fig. 1), are formed by silk screening a curable material such as the die attach adhesives discussed above. The chip or die 132 is then applied on the posts and the conductive material is cured. Leads 54 are applied by conventional bonding techniques such as conventional wire bonding. Spreader 60 is positioned above the front surface of the chip and a flowable, curable material is injected between the spreader and the dielectric element so that the curable liquid completely fills the spaces between the spreader 60 and dielectric element 20, including the spaces beneath chip 32, between posts 50. Complete filling, without voids, can be enhanced by application of pressure to the liquid during the filling process. For example, after application of the liquid but prior to curing, the assembly can be subjected to a pressure of about 10 to about 1000 pounds per square inch. As described in greater detail in copending, commonly assigned United States Patent Application 08/610,610, the disclosure of which is hereby incorporated by reference herein, application of such pressure can cause any voids which are initially present in a confined layer of liquid encapsulant to shrink and disappear. Although the present invention and the '610 application are not limited by any theory of operation, it is believed that such shrinkage results in part from dissolution of the gases contained in the voids in the liquid material. After the liquid material is applied, it is cured to form the lead encapsulant 58 and a rear encapsulant 52 of the same composition. In an alternative procedure, where a rear encapsulant 52 of different composition from the lead encapsulant 58 is desired, a liquid material adapted to form the rear

encapsulant is applied after posts 50 are cured but before bonds 54 are installed.

5 Numerous variations and combinations of the features discussed above may be utilized without departing from the present invention as defined by the claims. For example, the shape and configuration of the spreader may be varied as desired. The spreader may be provided with features such as fins to facilitate dissipation of heat from the spreader. Also, the spreader may be formed as a

10 "can" or "shroud" extending downwardly adjacent the edges of the dielectric element so that sidewalls of the spread protect the edges of the encapsulant-filled space. As shown in Fig. 5, posts 50 may be replaced by compliant thermal connectors as described in United States Patent No.

15 5,557,501, the disclosure of which is hereby incorporated by reference herein. Numerous flexible thermal conductors formed from elongated metallic strips as described in the '501 patent are interposed between the bottom surface 236 of the chip 234 and the top surface 222 of dielectric

20 element 220. As described in greater detail in the '501 patent, such thermal connectors can be formed by prefabricating striplike elements in flat configuration, connecting these elements between a pair of opposed elements and then moving the opposed elements away from one

25 another to bend the striplike elements into the desired curved, final configuration. A platelike carrier 237 may be provided with some of the flat striplike elements, whereas others of the flat striplike elements may be formed on the top surface 222 of dielectric element 220. The flat

30 striplike elements may be deformed to the curved configurations, to form the flexible thermal connectors 250 as depicted in Fig. 5 either before or after mounting chip 234 to platelike element 237.

00220" 64082960

The structure of Fig. 5 also has leads 254 provided as traces on a flexible dielectric sheet 253 similar to a conventional tape automated bonding or "TAB" tape. Leads 254 may be bonded to the contacts 240 of chip 234, and to bond points 256 on dielectric element 220 by processes such as employed in conventional TAB bonding. Where chip 234 is attached to platelike carrier 237 prior to the moving step discussed above, the TAB bonding step can be performed before the moving step, while platelike element 237 and chip 234 are positioned immediately above the dielectric element 220. Following this TAB bonding step, the chip may be moved away from dielectric element 220 so as to deform the striplike elements and form the thermal conductors 250 while also deforming the flexible tab tapes 253 to the condition illustrated in Fig. 5. Some "slack" may be provided in the TAB leads to accommodate this movement and bending, as by providing a fold or bend in the TAB tapes or the leads. Alternatively, the tab bonding step may be performed after positioning the chip in its final relationship to the dielectric element.

The spreader 260 depicted in Fig. 5 incorporates sidewalls 261 extending downwardly adjacent the edges of the package so as to protect the encapsulant 258 chip and leads from mechanical damage. In this embodiment, the same encapsulant 258 fills the entire package, including the spaces between thermally conductive elements 250, beneath chip 234.

Fig. 6 shows another embodiment of the present invention whereby the level of shear strain in the encapsulant in the vicinity of the contacts has been modified by changing the surface area of the spreader 360. For example, the spreader 360 shown in Fig. 6 is substantially smaller in surface area than the spreader 60 shown in Fig. 1 so that the encapsulant extends beyond the

spreader. Thus, the constraining force exerted by the spreader 360 is reduced, which in turn changes the shear stress in the encapsulant 358 in the vicinity of the contacts 340 on the chip 332. In alternative embodiments, the thermal mass of the spreader 360 may be modified to change the shear stress in the encapsulant 358 in the vicinity of the contacts 340.

Fig. 7 shows further embodiments for modifying the shear stress in the encapsulant. In these preferred embodiments, the shear stress is modified by changing the geometry or shape of the encapsulant layer 458. For example, in Fig. 7 the side walls 459 of the encapsulant 458 are sloped outwardly from the top to the bottom. Also, the spreader extends outwardly beyond the encapsulant at the top of the assembly. It is contemplated that other modifications to the geometry of the encapsulant are possible to modify the level of shear stress, e.g. concave sidewalls.

Fig. 8 shows a still further embodiment of the present invention which is similar to the assembly shown in Fig. 1 and described above; however, the assembly shown in Fig. 8 includes a layer 580 of a highly thermally conductive metal which is provided between the top surface 522 of the dielectric element 520 and the individual thermally conductive posts 550 disposed between the bottom surface of the chip 532 and the dielectric element 520. The highly conductive metal layer 580 preferably includes copper, however, other highly conductive metals may be utilized. The layer 580 preferably has a thickness between approximately one (1) to seven (7) mils. The thickness of the conductive metal layer 580 shown in Fig. 8 is greatly exaggerated for purposes of clarity. The highly conductive metal layer 580, which preferably overlies the top surface 522 of the dielectric element 520, provides enhanced

5

## WHAT IS CLAIMED IS:

1. A method of making a semiconductor chip assembly comprising the steps of:

5 (a) providing a dielectric element having top and bottom surfaces and terminals on said bottom surface;

(b) supporting semiconductor chip having a front surface with contacts thereon, a rear surface and edges extending between said front and rear surfaces above said  
10 top surface of said dielectric element by means of a plurality of posts extending between said rear surface of the chip and the top surface of the dielectric element; then

(c) applying a first curable liquid so that said  
15 first liquid penetrates between said rear surface and said top surface and penetrates between said posts; then

(d) curing said first liquid to form a flexible rear encapsulant;

(e) connecting said contacts to said terminals by  
20 connecting flexible leads between said contacts on said front surface and electrically conductive elements on said dielectric element; and

(f) providing a flexible lead encapsulant around said chip and said flexible leads.

25 2. A method as claimed in claim 1 wherein said step of providing a flexible lead encapsulant includes the steps of applying a second liquid of different composition from said first liquid and curing said second liquid.

30 3. A method as claimed in claim 2 wherein said step of applying said second liquid is performed after said step of curing said first liquid.

4. A method of making a semiconductor chip assembly comprising the steps of:

(a) providing a dielectric element having top and bottom surfaces and terminals on said bottom surface;

(b) supporting a semiconductor chip having a front surface with contacts thereon, a rear surface and edges extending between said front and rear surfaces above said top surface of said dielectric element by means of a plurality of posts extending between said rear surface of the chip and the top surface of the dielectric element; then

(c) connecting said contacts to said terminals by connecting flexible leads between said contacts on said front surface and electrically conductive elements on said dielectric element; and

(d) applying a first curable liquid so that said first liquid penetrates between said rear surface and said top surface and penetrates between said posts, and so that said first liquid surrounds said flexible leads; then

(e) curing said liquid to form a flexible rear encapsulant between the rear surface of the chip and the dielectric element and to form a flexible lead encapsulant integral with said rear around said chip and said flexible leads.

5. A method as claimed in claim 1 wherein said step of applying said first liquid includes the steps of placing said first liquid on said top surface of said dielectric element at edges of said chip and applying a gas under pressure around the chip and dielectric element to thereby force said first liquid into the spaces between said posts.

6. A method as claimed in claim 5 wherein said gas pressure is maintained during said step of curing said first liquid.

7. A method as claimed in claim 4 wherein said step of applying said first liquid includes the steps of

placing said first liquid on said top surface of said dielectric element at edges of said chip and applying a gas under pressure around the chip and dielectric element to thereby force said first liquid into the spaces between  
5 said posts.

8. A method as claimed in claim 7 wherein said gas pressure is maintained during said step of curing said first liquid.

9. A method of enhancing the reliability of  
10 electrical connections in a semiconductor package during operation of the chip, comprising the steps of:

(a) providing a semiconductor chip having a front contact bearing surface and a rear surface;

(b) providing flexible leads extending from said  
15 contacts on said front surface of said chip, said flexible leads being connected to said contacts at joints on said front surface;

(c) juxtaposing a spreader above said front surface, said spreader having a coefficient of thermal expansion substantially equal to the coefficient of thermal  
20 expansion of said chip; and

(d) disposing a liquid encapsulant between said front surface and said spreader and around said leads and curing said encapsulant, whereby the motion of the leads  
25 during thermal cycling leads is constrained.

10. The method as claimed in claim 9, further comprising the step of providing a predetermined geometry for the cured encapsulant so as to affect the constraintment of the leads.





FIG. 1

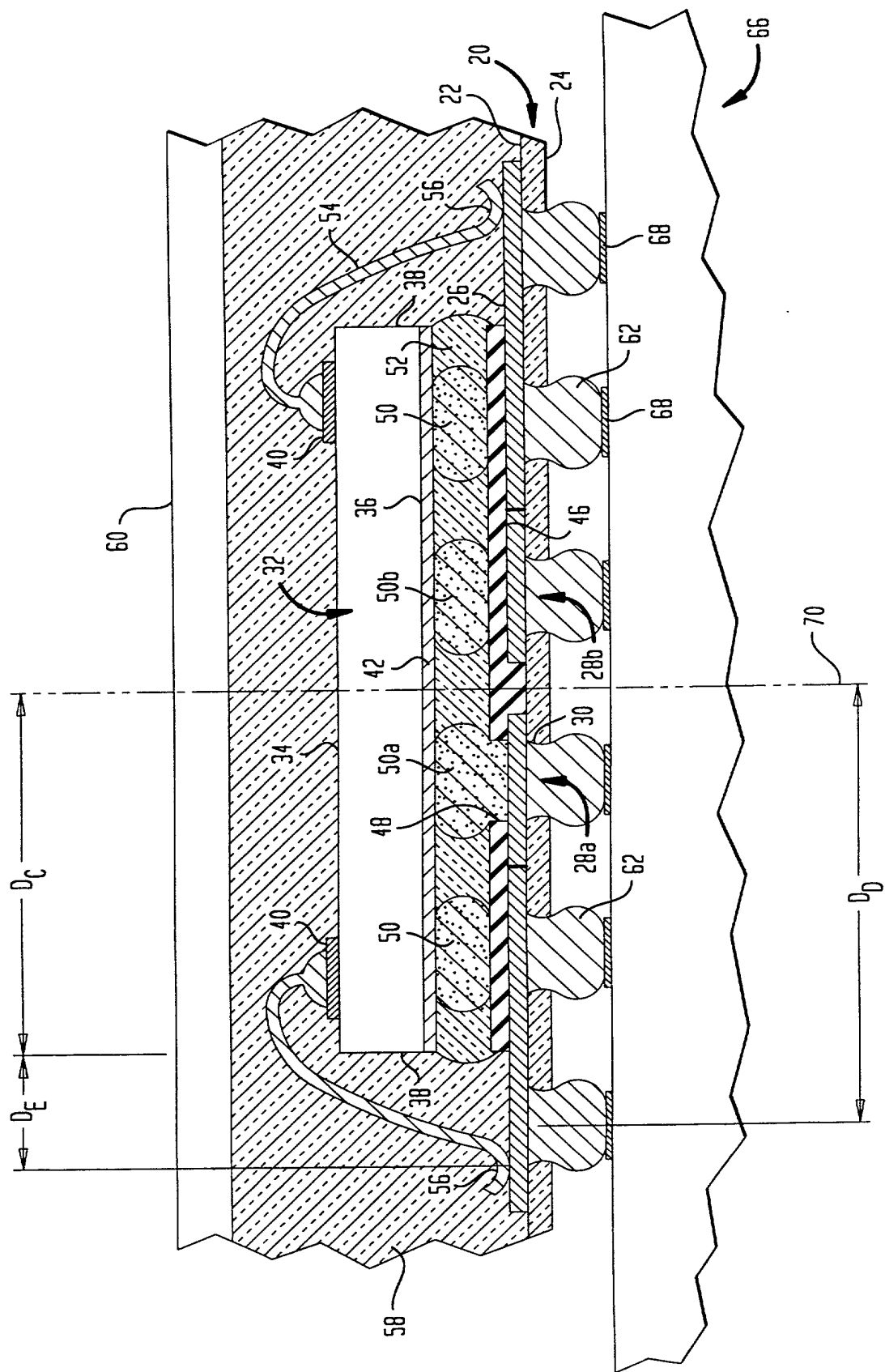


FIG. 2

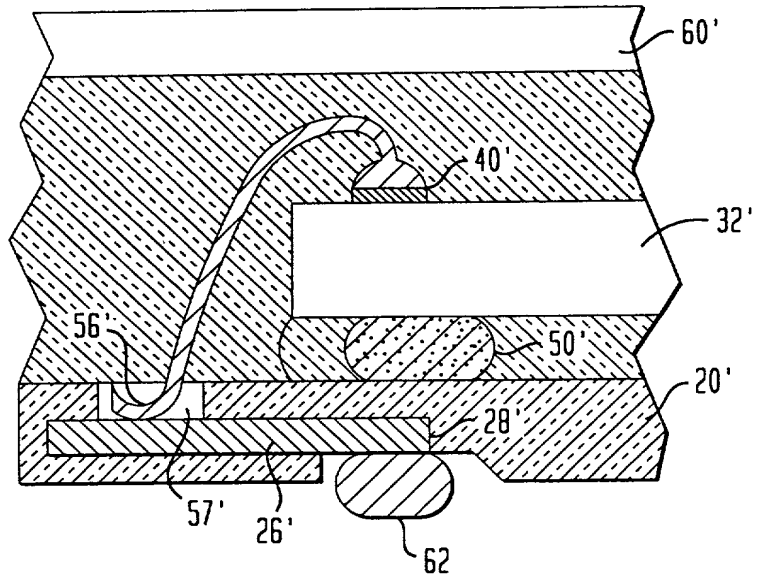


FIG. 3

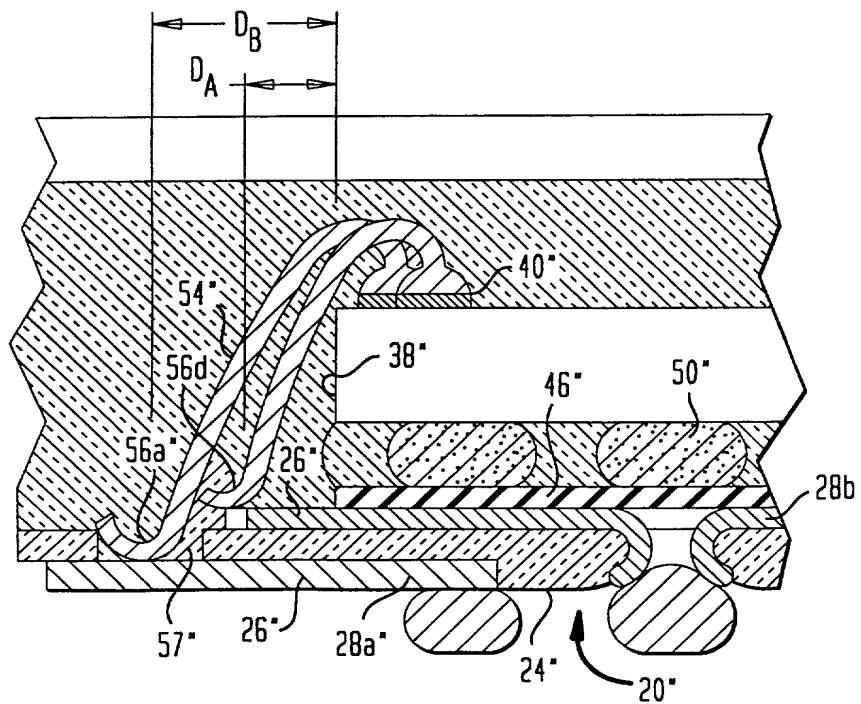




FIG. 5

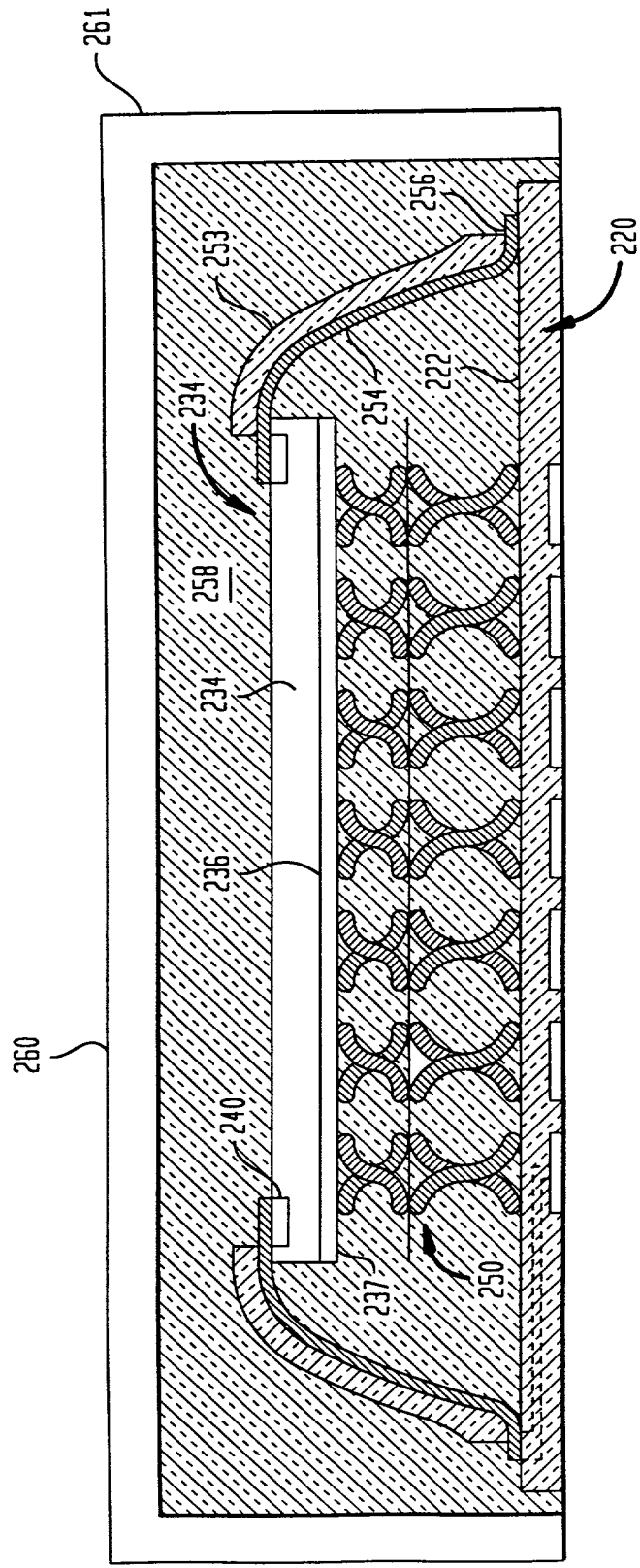
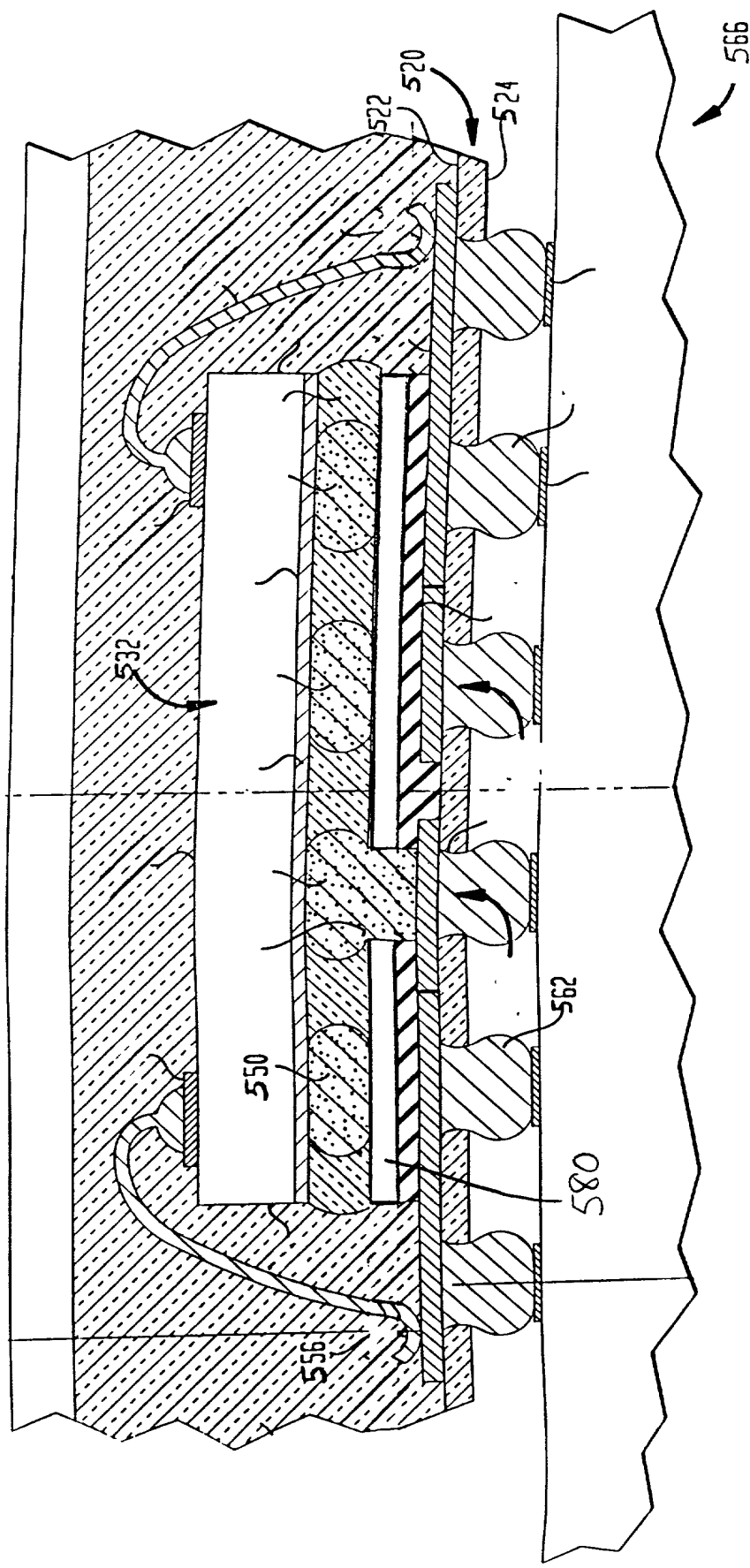




FIG. 8



# DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

ATTORNEY'S DOCKET NO.: TESSERA 3.0-102 II

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**PACKAGED MICROELECTRONIC ELEMENTS WITH ENHANCED THERMAL CONDUCTION** the specification of which

☐ is attached hereto

☒ was filed on October 31, 1997 as United States Application Number or PCT International Application Number 08/962,988 and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (month, day, year)	PRIORITY CLAIMED
			YES <input type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>

LISTING OF FOREIGN APPLICATIONS CONTINUED ON PAGE 3 HEREOF ☐ YES ☒ NO

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Application Number: 60/030,541 Filing Date: October 31, 1996

Application Number: 60/038,129 Filing Date: March 3, 1997

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Parent Application Serial Number:

Parent Filing Date:

Parent Patent No.:

U.S. Parent Application Serial Number:

Parent Filing Date:

Parent Patent No.:

PCT Parent Number:

Parent Filing Date:

LISTING OF US APPLICATIONS CONTINUED ON PAGE 3 HEREOF: ☐ YES ☒ NO

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Lawrence I. Lerner, Reg. No. 19,516; Sidney David, Reg. No. 22,768; Joseph S. Littenberg, Reg. No. 20,832; Arnold H. Krumholz, Reg. No. 25,428; William L. Mentlik, Reg. No. 27,108; John R. Nelson, Reg. No. 26,573; Roy H. Wepner, Reg. No. 28,350; Stephen B. Goldman, Reg. No. 28,512; Paul H. Kochanski, Reg. No. 29,660; Marcus J. Millet, Reg. No. 28,241; Bruce H. Sales, Reg. No. 32,793; Daniel H. Bobis, Reg. No. 16,694; Peter J. Butch III, Reg. No. 32,203; Keith E. Gilman, Reg. No. 32,137; Robert B. Cohen, Reg. No. 32,768; Arnold B. Dompieri, Reg. No. 29,736; Michael H. Teschner, Reg. No. 32,862; Jeffrey S. Dickey, Reg. No. 35,858; Gregory S. Gewirtz, Reg. No. 36,522; Jonathan A. David, Reg. No. 36,494; Shawn P. Foley, Reg. No. 33,071; Robert T. Canavan, Reg. No. 37,592; Michael J. Doherty, Reg. No. 40,592 and Christopher M. Pickett, Reg. No. 37,531.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature *Thomas H. Distefano* Date 3.11.98

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Second Inventor's signature \_\_\_\_\_ Date \_\_\_\_\_

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Third Inventor's signature \_\_\_\_\_ Date \_\_\_\_\_

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Fourth Inventor's signature \_\_\_\_\_ Date \_\_\_\_\_

Residence: \_\_\_\_\_ Citizenship: \_\_\_\_\_

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Full name of fifth joint inventor (given name, family name):

Fifth Inventor's signature \_\_\_\_\_ Date \_\_\_\_\_

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Full name of sixth joint inventor, if any (given name, family name):

Sixth Inventor's signature \_\_\_\_\_ Date \_\_\_\_\_

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Seventh Inventor's signature \_\_\_\_\_ Date \_\_\_\_\_

Residence: \_\_\_\_\_ Citizenship: \_\_\_\_\_

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Full name of eighth joint inventor, if any (given name, family name):

Eighth Inventor's signature \_\_\_\_\_ Date \_\_\_\_\_

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Post Office Address: \_\_\_\_\_

☐ Additional inventors are being named on separately numbered sheets attached hereto.